Project Report

ETS-26

L. E. Eaton

GEODSS ETS Computer/Hardware Configuration

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This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

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Group 94

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ABSTRACT

The GEODSS Experimental Test Site at White Sands, New Mexico is operating in the "duplex" mode now that the second telescope is on-line. The configuration of the two MODCOMP IV computers and peripherals is basic to the operation of two consoles and two telescopes. The report gives technical information on the computers and peripherals to explain how the direct memory processor interfaces external devices directly to memory.

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I. INTRODUCTION

This ETS Report describes the computer/hardware configuration of the present GEODSS ETS. This includes a block diagram of the system layout along with technical information for both ModComp computers. The technical information includes Device Addresses, Priorities, DMP Numbers, Controller Model Numbers and physical location of the equipment.

II. GENERAL DESCRIPTION

This Report is a technical description of the system configuration of the ModComp computers here at the GEODSS ETS. This information includes the following:

1. Physical layout of the computers
2. Peripheral devices on each computer
3. Model numbers of controllers for each peripheral device
4. I/O priorities of each peripheral
5. Data & Service interrupt locations for each peripheral
6. DMP information for applicable controllers
7. Technical information of interface between the computers and the Lincoln external logic
8. Block diagram of computer/peripheral/external logic configuration.

This Report becomes very important when considering system expansion or modification. The system expansion is limited by ModComp's ability to add peripherals. As is shown in this report, the ETS configuration is approaching its maximum capability.

Figures 1 and 2 of this Report show the physical layout of the two ModComp IV/25 computers and their peripheral controllers. Figure 3 is a block diagram of the computers, peripherals and ETS external components. Tables 1 and 2 give the technical software/hardware information for all the components of both computers.

III. DEFINITION OF TERMS

This section of the Report describes the definition of terms used in Tables 1 and 2 and the associated mnemonics.

A. HEX (#) - This is the standard symbol for a hexidecimal number. Since the ModComp is a 16 bit computer, the numbers are defined with the hex - "#" symbol.

B. DEVICE ADDRESS (DA) - ModComp uses a six bit code to describe up to 64_{10} devices that can be added to the system. Within the software instructions, these 64_{10} are broken into four GROUPS, each GROUP containing 16_{10} devices. They are -

GRP A = #00 - #0F DA's

GRP B = #10 - #1F DA's

GRP C = #20 - #2F DA's

GRP D = #30 - #3F DA's

Refering to ModComp's Reference Manual, an example of an Input Data Instruction = ID(A,B,C,D), RA, DA (in general); and for example, IDC,2,5 means, Input Data from Group C - to Register 2 - from device 5(#25).

C. INTERRUPT STRUCTURE (DI and SI)

ModComp uses 16_{10} external interrupts, (#0-#F). Interrupt level #0 being the highest. Each interrupt has a dedicated memory location for the software to put the starting location of the handler routine (called ENTRY), and a location that the CPU puts the current contents of the program counter in (called RETURN).

There are two external interrupt locations that are called I/O Party Line Data and Service Interrupts. These levels are vectored to 128_{10}

dedicated locations in core for ENTRY locations to Data and Service Interrupt routines. The I/O Party Line Data Interrupt (DI) level is #C and the I/O Party Line Service Interrupt (SI) level is #D. These party line interrupt structures are used by each controller.

The advantage of this scheme allows the hardware to have 128_{10} (64_{10} for DI and 64_{10} for SI) more interrupts. A problem arises if more than one of these interrupts occur at the same time. Since there is only one RETURN location (say, for SI, level #D), there has to be some scheme for the hardware to decide which Party Line Interrupt is serviced. This is handled by the I/O priority structure. The controller with the highest priority is allowed to be serviced first. For more detailed analysis, refer to ModComp's Reference Manual.

The Data Interrupt (DI) and Service Interrupt (SI)entry locations are given in Tables 1 and 2. A rule of thumb for the entry location is given by: DI = #80 + DA of the Controller

SI = #C0 + DA of the Controller

For example, the DA of the Interval Timer = #1F; therefore, the DI entry location is: DI(Interval Timer) = #80 + #1F = #9F.

D. I/O PRIORITY STRUCTURE (PRIOR) - ModComp's I/O Priority Structure is used to determine which controller receives an I/O interrupt Service if one or more controllers are interrupting the CPU at the same time. This is for the two I/O priority interrupts, which are external interrupt level #D (Service Interrupt) and #C (Data Interrupt). There are seventeen priority levels and these seventeen levels actually determine how many controllers each machine can have. That is, each

machine can have up to seventeen peripheral controllers that use I/O priority interrupts.

The above analysis is a bit confusing because, for example, the I/101S has an I/O priority of #6, but there are 16_{10} channels associated with this one priority. The interrupts of these 16_{10} channels are internally prioritied within the I/01S.

In general then, even though there can be up to 64_{10} device addresses on the system, the ModComp is basically restricted to the number of I/O Priorities. Our system has almost reached that limit now.

An I/O Priority of 0 is the highest and 16_{10} is the lowest. Table 1 and 2 give the priorities of the A and B computers respectively.

E. DIRECT MEMORY PROCESSOR (DMP)

The DMP is ModComp's way of allowing external devices to interface directly to memory. This is analogous to other computers' DMA channels. We have two controllers built by Lincoln that use this. They are the Vector General and the Gallium Arsenide Photometer.

The software is required to tell the hardware where to start loading data into core (for input mode) and how many words are to be transferred. This is done by loading two words into dedicated location of core. One is the Transfer Address (TA) which is the starting location of data transfer and the other is Transfer Count (TC) which is the two's complement of the length of data to be transferred.

There are dedicated locations in Core from which each DMP controller

obtains the TA and TC. These locations are given in Tables 1 and 2.

A rule of thumb for these core locations is:

TC = #60 + DMP Nos.

TA = #70 + DMP Nos.

For example, the Vector General's DMP No. is #02. Thus -

TC (Vect. Gen.) = #60 + #02 = #62.

TA (Vect. Gen.) = #70 + #02 = #72.

IV. TABLES AND FIGURES

Figures 1 and 2 show the physical layout of the A and B ModComps respectively. They show the location of the various controllers and racks.

Figure 3 is the block diagram of the computer/hardware configuration.

Tables 1 and 2 give the pertinent technical information of the A and B ModComps respectively. This includes DA PRIOR, DI, SI, TA, TC, GRP, Model Nos., DMP Nos, Bus and description.

MODCOMP IV - SYSTEM A

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I/OIS - 2	I/OIS - 1	MT 2	MT 1	MODAC DA = #30-3B PRI = 13 DMP = 5	CPU
		I/OIS SW #1 DA = 6 PRI = 9 I/OIS SW #2 DA = 9 PRI = 10	PCI 1-A BUS = PIOP DRV/RCD ½ PLN TTY(3751) ½ PLN DA = #0A PRI = 15 INTV T(4701)½ PLN DA = #1F PRI = 2 ASY COM(4811)½PLN DA = #18/#19 PRI = 3 ASY COM(4811)½PLN DA = #1A/#1B PRI = 4	PCI 2-A BUS = SIOP DRV/RCV ½ PLN MHD(4132) 1 PLN DA = #01 PRI = 01 DMP = 1 MTU(4148) 1 PLN DA = #04 PRI = 7 DMP = 4 COM-COM LINK(4820) ½ PLN DA = #03 PRI = 1 DMP = 03	
AICN - 2 B - SYSTEM	AICN - 1 A - SYSTEM				

Fig. 1. System A, physical location of controllers with DA, PRI, DMP, model nos, and physical plane size.

MODCOMP IV - SYSTEM B

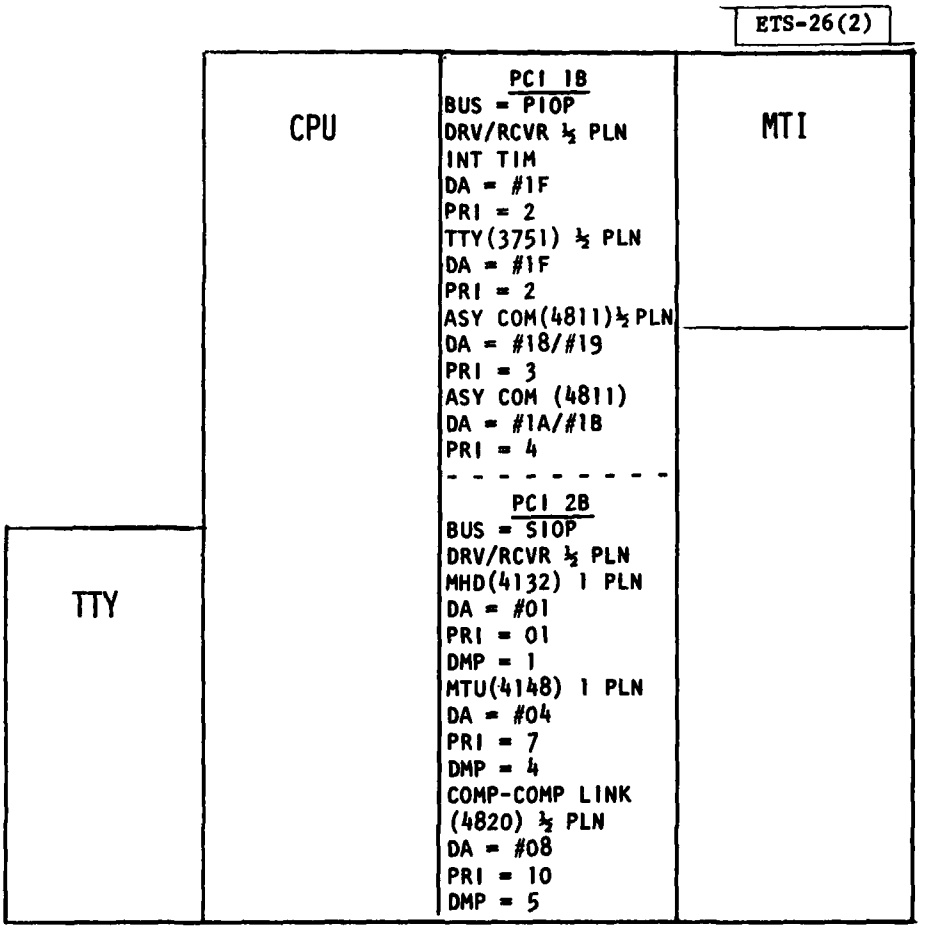

Fig. 2. System B, physical location of controllers with DA, PRI, DMP, model nos, and physical plane size.

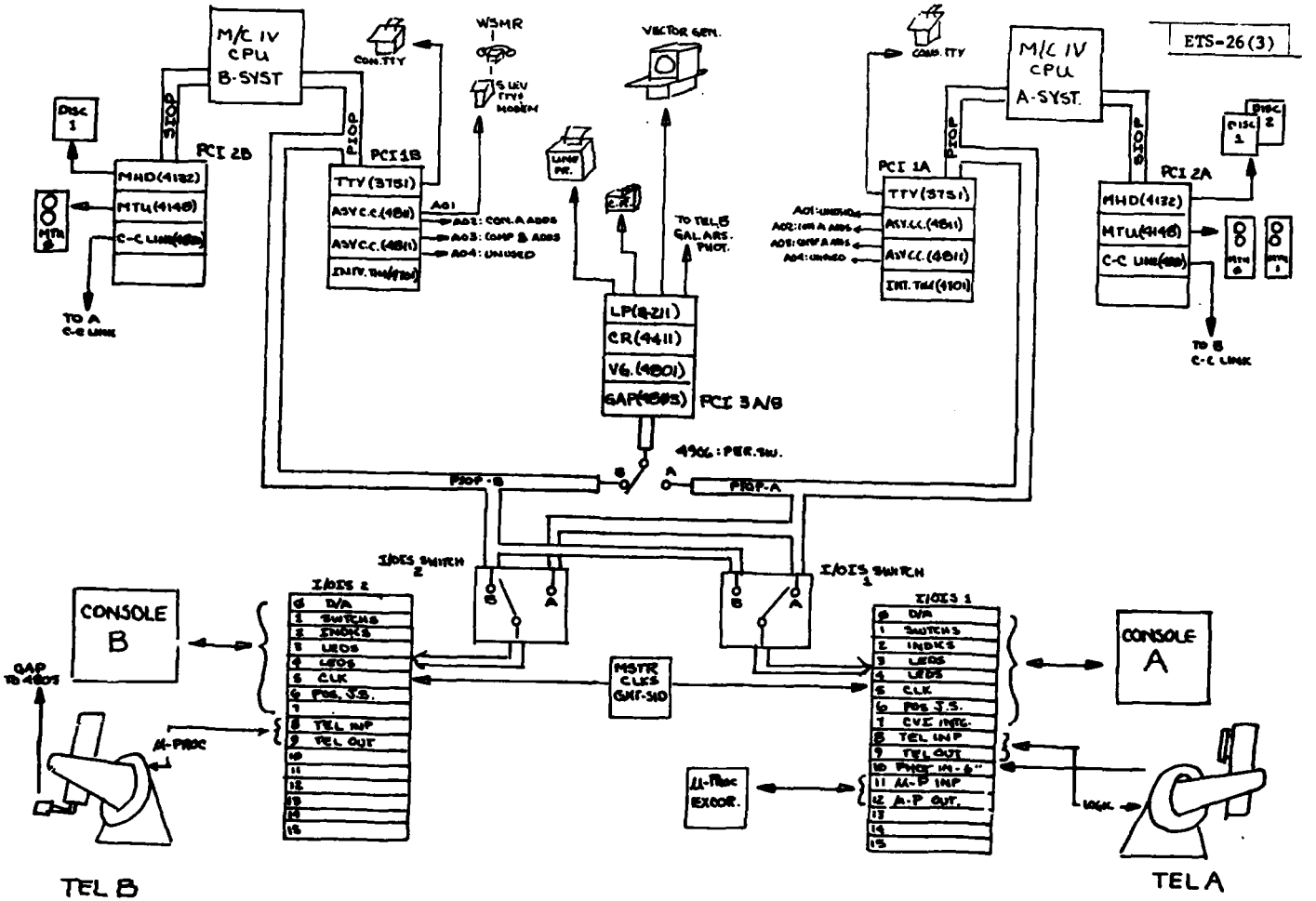

Fig. 3. GEODSS computer/system block diagram

TABLE 1

PERIPHERAL DEVICE INFORMATION - SYSTEM A

I/O PRIOR	INTRPT LOC(#) DI	INTRPT LOC(#) SI	DMP LOC(#) TC	DMP LOC(#) TA	DEV ADDR #	DMP NOS	SOFT WARE DESIG	GROUP	BUS	PCI NOS	MODEL NOS	PERIPHERAL DEVICE DESCRIPTION
0	83	C3	63	73	03	3	-	A	SIOP	2A	4820	Computer-Computer Link
1	81	C1	61	71	01	1	M0 & M1	A	SIOP	2A	4132	Moving Head Disc (2)
2	9F	DF	--	--	1F	-	-	B	PIOP	1A	4701	Interval Timer
3	98	D8	--	--	18	-	A01 &	B	PIOP	1A	4811	Output Asy Comm Ctrlr
	99	D9	--	--	19	-	A02					Input A01-unused; A02-Console ADDS A System
4	9A	DA	--	--	1A	-	A03 &	B	PIOP	1A	4811	Output Asy Comm Ctrlr
	9B	DB	--	--	1B	-	A04					Input A03-Comp ADDS; A04 -unused A System
5	82	C2	62	72	02	2	-	A	PIOP	3A/B	4801	Vector General
6	A0	E0	--	--	20	-	-	C	PIOP	-	I/OIS	Ch 0: D/A 2Chan Chan 1 = SCR Chan 2 = Unused
	A1**	E1	--	--	21	-	-	C	PIOP	-	I/OIS	Ch 1: Switch Input (AICN-1)
	A2**	E2	--	--	22	-	-	C	PIOP	-	I/OIS	Ch 2: Indic Output (AICN-2)
	A3	E3	--	--	23	-	-	C	PIOP	-	I/OIS	Ch 3: Display Leds (AICN-3)
	A4	E4	--	--	24	-	-	C	PIOP	-	I/OIS	Ch 4: Display Leds (AICN-4)
	A5	E5	--	--	25	-	-	C	PIOP	-	I/OIS	Ch 5: Mstr Clks-Input (AICN-5)
	A6	E6	--	--	26	-	-	C	PIOP	-	I/OIS	Ch 6: Posit Joystk-Input (AICN-6)
	A7*	E7	--	--	27	-	-	C	PIOP	-	I/OIS	Ch 7: CVI Integ-Input (AICN-7)
	--	--	--	--	28	-	-	C	PIOP	-	I/OIS	Ch 8: Tele A-Input (AICN-8)
	--	--	--	--	29	-	-	C	PIOP	-	I/OIS	Ch 9: Tele A-Output (AICN-9)
	--	--	--	--	2A	-	-	C	PIOP	-	I/OIS	Ch 10: 6" Photom.-Input (AICN-10)
	--	--	--	--	2B	-	-	C	PIOP	-	I/OIS	Ch 11: M-Proc.-Input (AICN-11)
	--	--	--	--	2C	-	-	C	PIOP	-	I/OIS	Ch 12: M-Proc.-Output (AICN-12)
	--	--	--	--	2D	-	-	C	PIOP	-	I/OIS	Ch 13: unused
	--	--	--	--	2E	-	-	C	PIOP	-	I/OIS	Ch 14: unused
	--	--	--	--	2F	-	-	C	PIOP	-	I/OIS	Ch 15: unused

* S0: Interrupt

** A1 = M-Proc Input Interrupt (AICN-11)

** A2 = M-Proc Output Interrupt (AICN-12)

TABLE 1 (Continued)

I/O PRIOR.	INTRPT LOC(#)		DMP LOC(#)		DEV ADDR #	DMP NOS	SOFT WARE DESIG	GROUP	BUS	PCI NOS	MODEL NOS	PERIPHERAL DEVICE DESCRIPTION
7	84	C4	64	74	04	4	MT1&2	A	S1OP	2A	4148	Mag Tape (2)
8	85	C5	--	--	05	-	-	A	P1OP	3A/B	4411	Card Reader
9	86	C6	--	--	06	-	-	A	P1OP	-	-	I/OIS Switch #1 A System
10	89	C9	--	--	09	-	-	A	P1OP	-	-	I/OIS Switch #2 B System
11	87	C7	--	--	07	-	LP	A	P1OP	3A/B	4211	Line Printer
12	90	C0	--	--	10	-	-	B	P1OP	3A/B	4906	Peripheral Switch
13*	80	F0	--	--	30	5	-	D	P1OP	-	16XX	Modac-Analog Input:Weather, Camera, SOI
14	88	C8	66	76	08	6	-	A	P1OP	3A/B	4805	Gall Ars Photometer
15	8A	CA	--	--	0A	-	TY	A	P1OP	1A	3751	Console TTY
16												Unused

* The Modac can use DA's of 30-3B and interrupts of SI = B0-BB, DI = F0-FB. This system uses only DA = 30.

TABLE 2

PERIPHERAL DEVICE INFORMATION - SYSTEM B

I/O	INTRPT LOC(#)		DMP LOC(#)		DEV ADDR #	DMP NOS	SOFT WARE DESIG	GROUP	BUS	PCI NOS	MODEL NOS	PERIPHERAL DEVICE DESCRIPTION
	DI	SI	TC	TA								
0	83	C3	63	73	03	3	-	A	SIOP	2B	4820	Computer-Computer Link
1	81	C1	61	71	01	1	M0 & M1	A	SIOP	2B	4132	Moving Head Disc (2)
2	9F	DF	--	--	1F	-	-	B	PIOP	1B	4701	Interval Timer
3	98	D8	--	--	18	-	A01 & A02	B	PIOP	1B	4811	Output Asy Comm Ctrlr Input A01-unused; A02-Console ADDS B System
	99	D9	--	--	19	-						
4	9A	DA	--	--	1A	-	A03 & A04	B	PIOP	1B	4811	Output Asy Comm Ctrlr Input A03-Comp ADDS; A04-unused
5	82	C2	62	72	02	2	-	A	PIOP	3A/B	4801	Vector General
6	A0	E0	--	--	20	-	-	C	PIOP	-	I/OIS	Ch 0:D/A 2 Chan Chan 1 = SCR Chan 2 = Unused
	A1	E1	--	--	21	-	-	C	PIOP	-	I/OIS	Ch 1: Switch Input (AICN-1)
	A2	E2	--	--	22	-	-	C	PIOP	-	I/OIS	Ch 2: Indic Output (AICN-2)
	A3	E3	--	--	23	-	-	C	PIOP	-	I/OIS	Ch 3: Display Leds (AICN-3)
	A4	E4	--	--	24	-	-	C	PIOP	-	I/OIS	Ch 4: Display Leds (AICN-4)
	A5	E5	--	--	25	-	-	C	PIOP	-	I/OIS	Ch 5: Mstr Clks-Input (AICN-5)
	A6	E6	--	--	26	-	-	C	PIOP	-	I/OIS	Ch 6: Post Joystk-Input (AICN-6)
	A7	E7	--	--	27	-	-	C	PIOP	-	I/OIS	Ch 7:
	--	--	--	--	28	-	-	C	PIOP	-	I/OIS	Ch 8: Tele B Input (AICN-8B)
	--	--	--	--	29	-	-	C	PIOP	-	I/OIS	Ch 9: Tele B Output (AICN-9B)
	--	--	--	--	2A	-	-	C	PIOP	-	I/OIS	Ch 10: unused
	--	--	--	--	2B	-	-	C	PIOP	-	I/OIS	Ch 11: unused
	--	--	--	--	2C	-	-	C	PIOP	-	I/OIS	Ch 12: unused
	--	--	--	--	2D	-	-	C	PIOP	-	I/OIS	Ch 13: unused
	--	--	--	--	2E	-	-	C	PIOP	-	I/OIS	Ch 14: unused
	--	--	--	--	2F	-	-	C	PIOP	-	I/OIS	Ch 15: unused

TABLE 2 (Continued)

I/O PRIOR	INTRPT LOC (#) DI	SI	DMP LOC (#) TC	TA	DEV ADDR #	DMP NOS	SOFT WARE DESIG	GROUP	BUS	PCI NOS	MODEL NOS	PERIPHERAL DEVICE DESCRIPTION
7	84	C4	64	74	04	4	MT1&2	A	SIOP	2B	4148	Mag Tape (2)
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11	87	C7	--	--	07	-	LP	A	PIOP	3A/B	4211	Line Printer
12	90	C0	--	--	10	-	-	B	PIOP	3A/B	4906	Peripheral Switch
13												Unused
14	88	C8	66	76	18	6	-	A	PIOP	3A/B	4805	Gall Ars Photometer
15	8A	CA	--	--	0A	-	TY	A	PIOP	1B	3751	Console TTY
16												Unused

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